**Cell Description:**

This is a standard buffer cell with the following Boolean equation.

Each buffer is constructed by two inverters in series. To compensate for rise and fall times the input inverter is scaled appropriately by required drive strength of the output. In this cell library the both the BUFX2 and BUFX4 are driven by an inverter with a drive strength of 1, and the BUFX8 is driven by an invert with a drive strength of 2.

**Truth Table:**

|  |  |
| --- | --- |
| A | Y |
| 0 | 0 |
| 1 | 1 |

**Behavioral Verilog:**The behavioral Verilog for the inverter is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2, and 4).

//Verilog HDL for "Lib6710\_06", "BUFX2" "behavioral"

module BUFX2 ( Y, A );

input A;

output Y;

buf \_i0(Y,A);

specify

(A => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| BUFFX2 | 27.0 | 7.2 |
| BUFFX4 | 27.0 | 7.2 |
| BUFFX8 | 27.0 | 9.6 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Logic Symbol:**

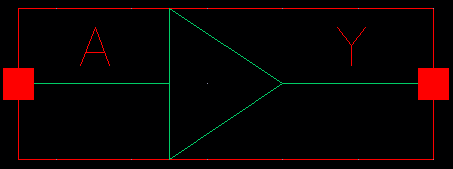
****

Figure 1: Symbol View for the buffer cell.

**CMOS Schematic:**The following figures display the CMOS schematics for the BUF cells.

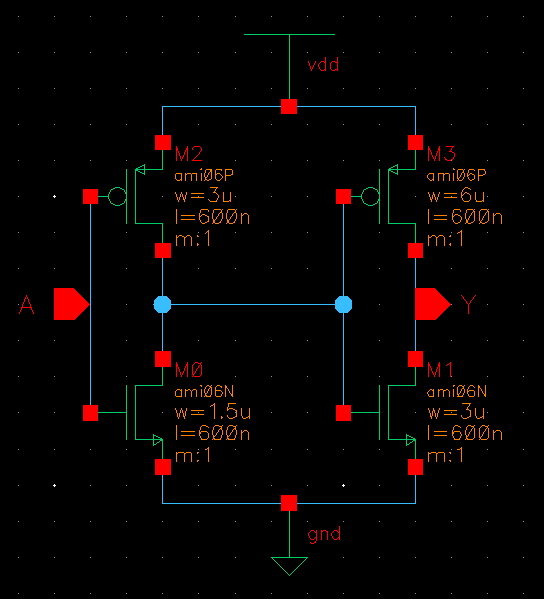
****

Figure 2: CMOS Schematic for the BUFX2 cell.

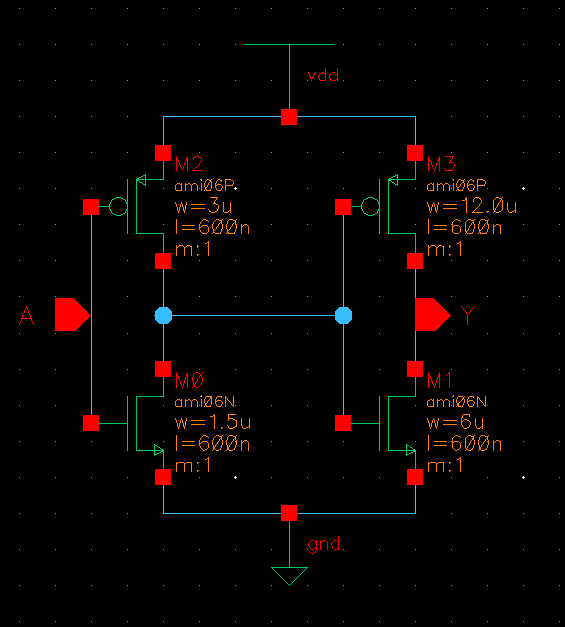


Figure 3: CMOS Schematic for the BUFX2 cell.

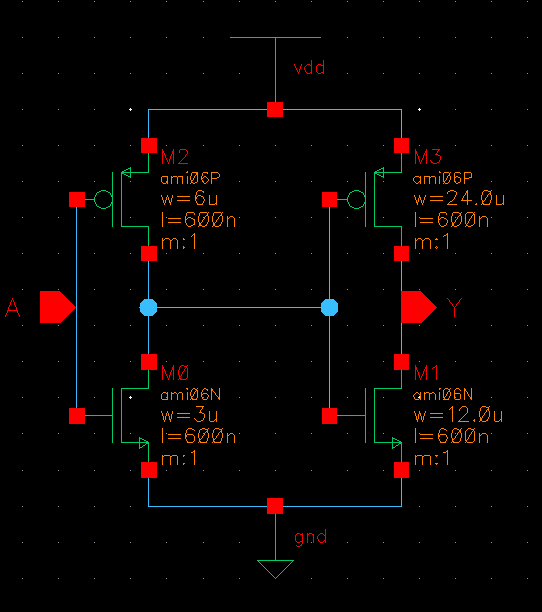


Figure 4: CMOS Schematic for the BUFX8 cell.

**CMOS Layout:**

The following figures display the CMOS layouts for the BUF cells.

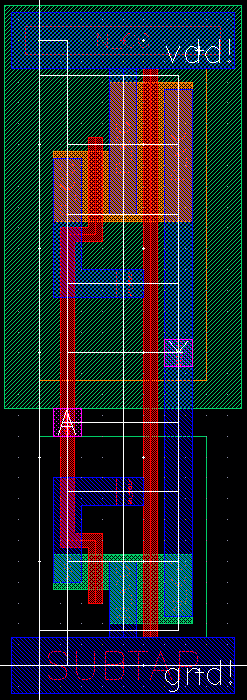
****

Figure 5: CMOS layout for the BUFX2 cell.

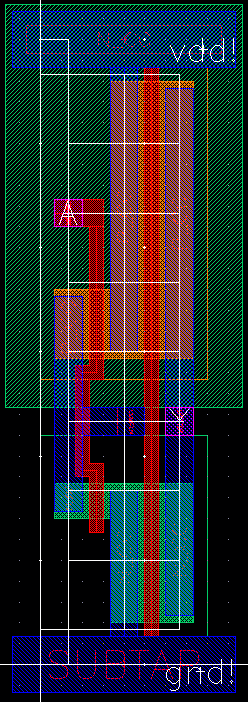
****

Figure 6: CMOS layout for the BUFX4 cell.

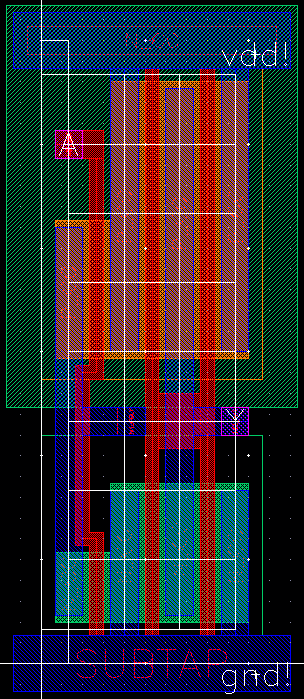
****

Figure 7: CMOS layout for the BUFX8 cell.